



# M5L27512K, -17, -2

**524288-BIT (65536-WORD BY 8-BIT)  
ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

## DESCRIPTION

The Mitsubishi M5L27512K is a high-speed 524288 bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5L27512K is fabricated by N-channel double polysilicon gate technology and is available in a 28-pin DIP with a transparent lid.

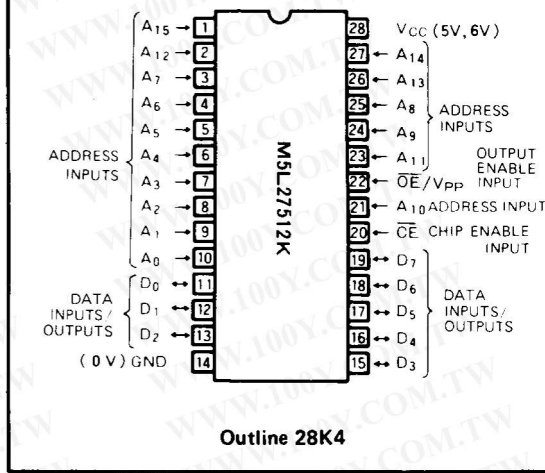
## FEATURES

- 65536 Word x 8 bit organization
- Access time M5L27512K-17 . . . . . 170ns (max.)  
M5L27512K-2 . . . . . 200ns (max.)  
M5L27512K . . . . . 250ns (max.)
- Programming voltage: 12.5V
- Two line control  $\overline{OE}$ ,  $\overline{CE}$
- Lower power current ( $I_{CC}$ ): Active . . . 100mA (max.)  
Stand by . . . 40mA (max.)
- Single 5V power supply
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 28-pin DIP
- Fast programming algorithm

## APPLICATION

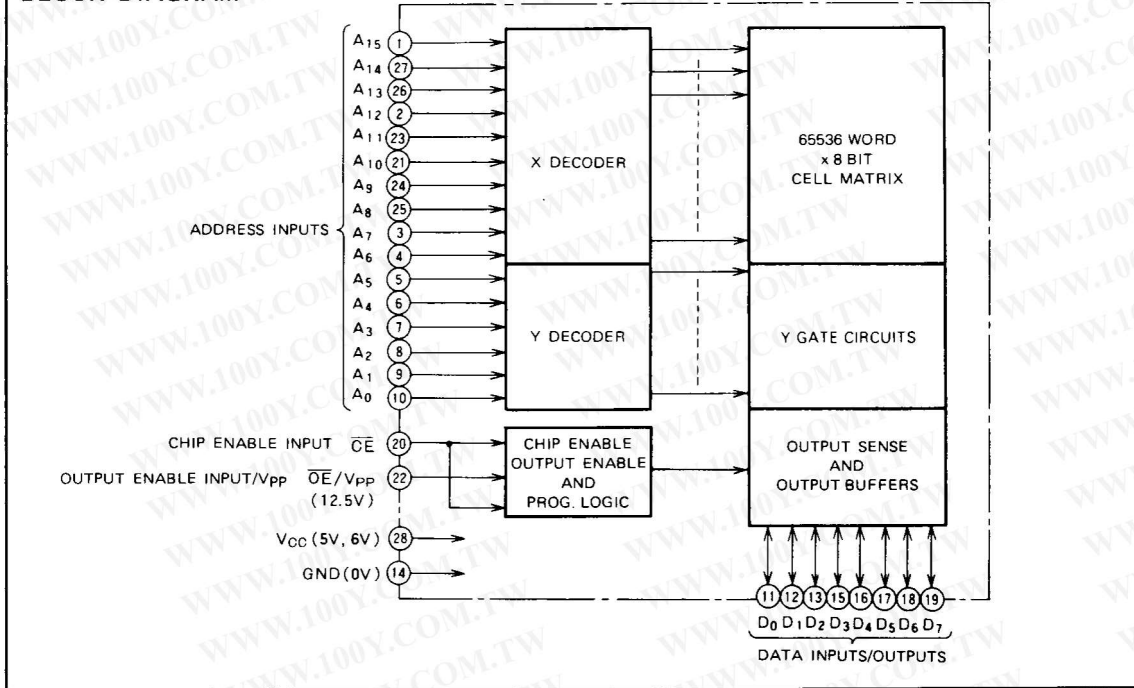
Microcomputer systems and peripheral equipment

## PIN CONFIGURATION (TOP VIEW)



**勝特力材料 886-3-5753170**  
**勝特力电子(上海) 86-21-54151736**  
**勝特力电子(深圳) 86-755-83298787**  
[Http://www.100y.com.tw](http://www.100y.com.tw)

## BLOCK DIAGRAM



**524288-BIT (65536-WORD BY 8-BIT)  
 ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

**FUNCTION**

**Read**

Set the  $\overline{CE}$  and  $\overline{OE}/V_{PP}$  terminals to the read mode (low level). Low level input to  $\overline{CE}$  and  $\overline{OE}/V_{PP}$  and address signals to the address inputs ( $A_0 \sim A_{15}$ ) make the data contents of the designated address location available at the data input/output ( $D_0 \sim D_7$ ). When the  $\overline{CE}$  or  $\overline{OE}/V_{PP}$  signal is high, data input/output are in a floating state.

When the  $\overline{CE}$  signals is high, the device is in the standby mode or power-down mode.

**Programming**

**(Fast programming algorithm)**

First set  $V_{CC} = 6V$ ,  $\overline{OE}/V_{PP} = 12.5V$  and then set an address to first address to be programmed. After applying 1ms program pulse ( $\overline{CE}$ ) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 1ms program pulse. The programmer continues 1ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 1ms pulses applied to that address in register X. And then applied a program pulse 3 times of register X value long as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed.

**Erase**

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of approximately 15WS/cm<sup>2</sup>. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.

勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-54151736  
 勝特力电子(深圳) 86-755-83298787  
 Http://www.100y.com.tw

**MODE SELECTION**

Mode	Pins	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	$V_{CC}$ (28)	Outputs (11 ~ 13, 15 ~ 19)
Read		$V_{IL}$	$V_{IL}$	5 V	Data out
Output disable		$V_{IL}$	$V_{IH}$	5 V	Floating
Standby		$V_{IH}$	X*	5 V	Floating
Program		$V_{IL}$	12.5V	6 V	Data in
Program inhibit		$V_{IH}$	12.5V	6 V	Floating

\*: X can be either  $V_{IL}$  or  $V_{IH}$

**ABSOLUTE MAXIMUM RATINGS** (Note 1)

Symbol	Parameter	Ratings	Unit
$T_{opr}$	Operating temperature	-10 ~ 80	°C
$T_{stg}$	Storage temperature	-65 ~ 125	°C
$V_{I1}$	All input or output voltage (Note 2)	-0.6 ~ 7.0	V
$V_{I2}$	$\overline{OE}/V_{PP}$ supply voltage (Note 2)	-0.6 ~ 14.0	V
$V_{I3}$	A9 input voltage (Note 2)	-0.6 ~ 13.5	V

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

2: With respect to Ground.

# M5L27512K, -17, -2

## 524288-BIT (65536-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### READ OPERATION

#### DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0~70°C, V<sub>CC</sub> = 5V ± 5%, unless otherwise noted)

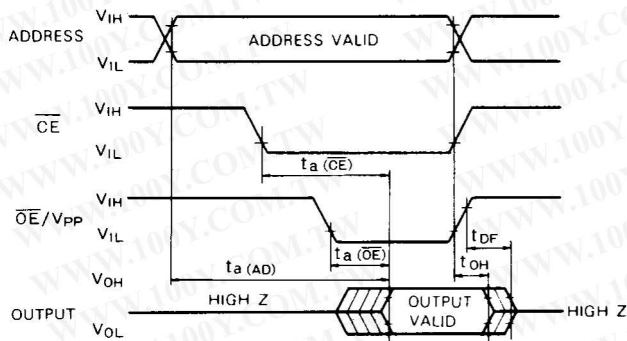
Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
I <sub>LI</sub>	Input leakage current	V <sub>IN</sub> = 5.5V			10	μA
I <sub>LO</sub>	Output leakage current	V <sub>OUT</sub> = 5.5V			10	μA
I <sub>CC1</sub>	V <sub>CC</sub> current standby	$\overline{CE} = V_{IH}$			40	mA
I <sub>CC2</sub>	V <sub>CC</sub> current active	$\overline{CE} = \overline{OE}/V_{PP} = V_{IL}$			100	mA
V <sub>IL</sub>	Input low voltage		-0.1		0.8	V
V <sub>IH</sub>	Input high voltage		2.0		V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 2.1mA			0.45	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = -400μA	2.4			V

Note 3: Typical values are at T<sub>a</sub> = 25°C and nominal supply voltages.

#### AC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0~70°C, V<sub>CC</sub> = 5V ± 5%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M5L27512K-17		M5L27512K-2		M5L27512K		
			Min	Max	Min	Max	Min	Max	
t <sub>a</sub> (AD)	Address to output delay	$\overline{OE} = \overline{OE}/V_{PP} = V_{IL}$		170		200		250	ns
t <sub>a</sub> ( $\overline{CE}$ )	$\overline{CE}$ to output delay	$\overline{OE}/V_{PP} = V_{IL}$		170		200		250	ns
t <sub>a</sub> ( $\overline{OE}$ )	$\overline{OE}$ to output delay	$\overline{CE} = V_{IL}$		60		75		100	ns
t <sub>DF</sub>	$\overline{OE}$ high to output float	$\overline{CE} = V_{IL}$	0	50	0	60	0	60	ns
t <sub>OH</sub>	Output hold from $\overline{CE}$ , $\overline{OE}$ or addresses		0		0		0		ns

### AC WAVEFORMS



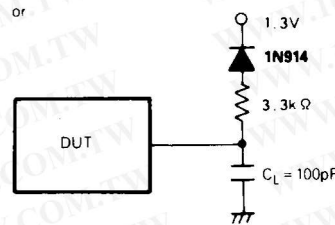
Test conditions for A.C. characteristics

Input voltage: V<sub>IL</sub> = 0.45V, V<sub>IH</sub> = 2.4V

Input rise and fall times: ≤ 20ns

Reference voltage at timing measurement: Input 0.8V and 2V Output 0.8V, and 2V.

Output load: 1TTL gate + C<sub>L</sub> (100pF)



### CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>IN</sub>	Input capacitance	T <sub>a</sub> = 25°C, f = 1MHz, V <sub>I</sub> = V <sub>O</sub> = 0V		4	6	pF
C <sub>OUT</sub>	Output capacitance			8	12	pF
C <sub><math>\overline{OE}/V_{PP}</math></sub>	$\overline{OE}/V_{PP}$ Input capacitance			30	40	pF

**M5L27512K, -17, -2****524288-BIT (65536-WORD BY 8-BIT)  
ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM****PROGRAM OPERATION****FAST PROGRAMMING ALGORITHM  
DC ELECTRICAL CHARACTERISTICS**

(Ta = 25 ± 5 °C, VCC = 6V ± 0.25V, Vpp = 12.5V ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>LI</sub>	Input current	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>			10	μA
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 2.1mA			0.45	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = 400μA	2.4			V
V <sub>IL</sub>	Input low voltage		0.1		0.8	V
V <sub>IH</sub>	Input high voltage		2.0		V <sub>CC</sub>	V
I <sub>CC2</sub>	V <sub>CC</sub> supply current				100	mA
I <sub>PP2</sub>	OE/Vpp supply current	CE = V <sub>IL</sub>			50	mA

**AC ELECTRICAL CHARACTERISTICS** (Ta = 25 ± 5 °C, VCC = 6V ± 0.25V, Vpp = 12.5V ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>AS</sub>	Address setup time		2			μs
t <sub>OES</sub>	OE/Vpp setup time		2			μs
t <sub>OEH</sub>	OE/Vpp hold time		2			μs
t <sub>DS</sub>	Data setup time		2			μs
t <sub>AH</sub>	Address hold time		0			μs
t <sub>DH</sub>	Data hold time		2			μs
t <sub>DFP</sub>	CE to output float delay		0		130	ns
t <sub>VCS</sub>	V <sub>CC</sub> setup time		2			μs
t <sub>FPW</sub>	CE initial program pulse width		0.95	1.0	1.05	ms
t <sub>OPW</sub>	CE over program pulse width		2.85		78.75	ms
t <sub>DV</sub>	Data valid from CE				1	μs
t <sub>VR</sub>	OE/Vpp recovery time		2			μs
t <sub>PRT</sub>	OE/Vpp pulse rise time during program		50			ns

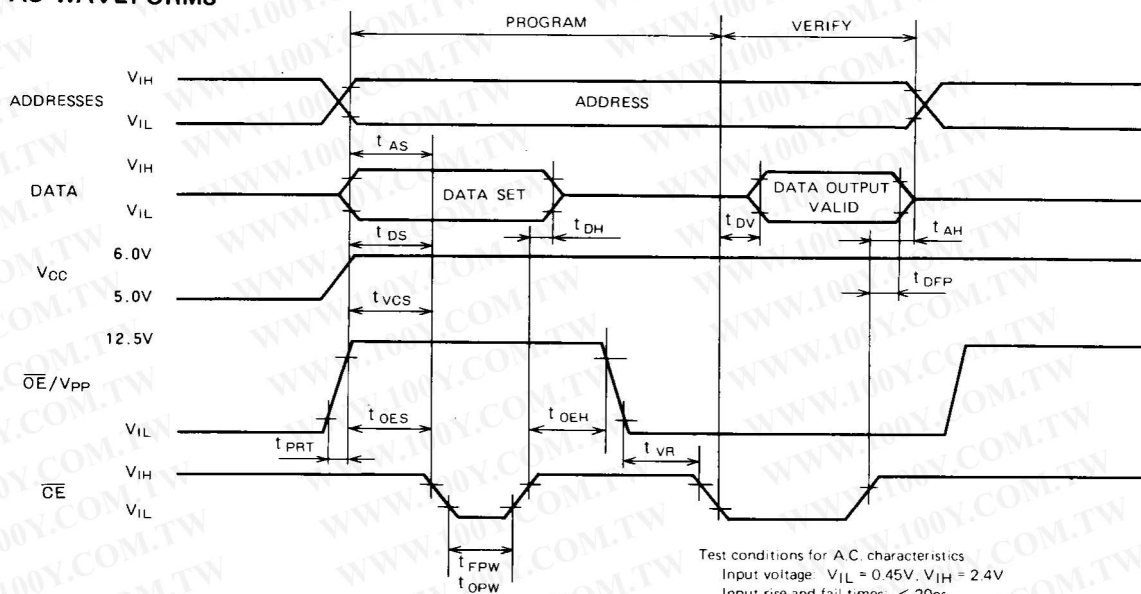
Note 4: V<sub>CC</sub> must be applied simultaneously or before OE/Vpp and removed simultaneously or after OE/Vpp.

勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-54151736  
 勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

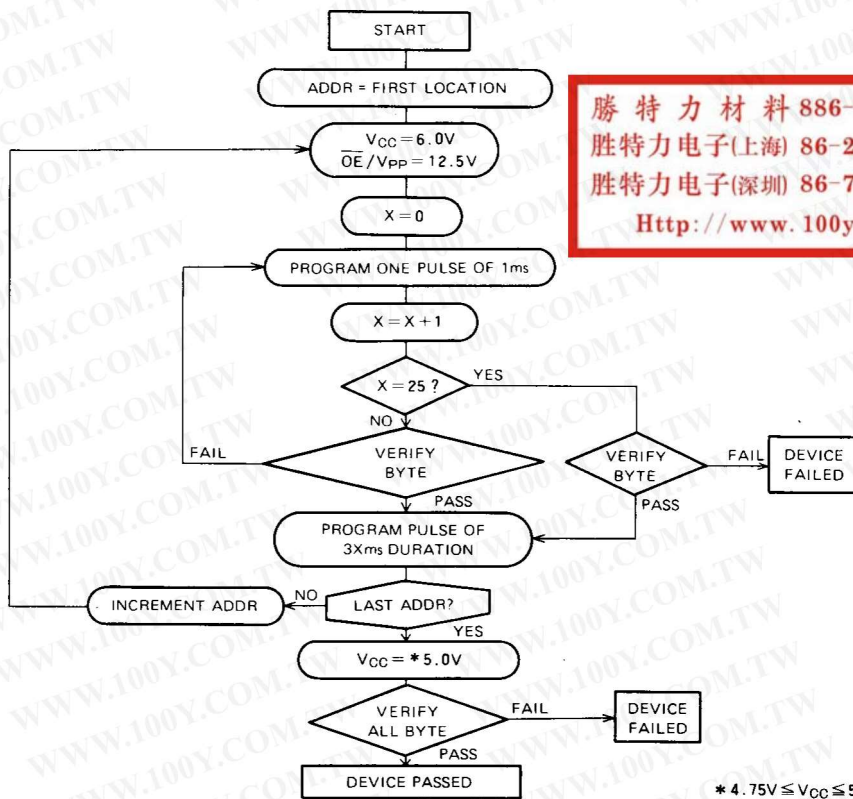
# M5L27512K, -17, -2

## 524288-BIT (65536-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### AC WAVEFORMS



### FAST PROGRAMMING ALGORITHM FLOW CHART



勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-54151736  
 勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)

\*  $4.75V \leq V_{CC} \leq 5.25V$



**524288-BIT (65536-WORD BY 8-BIT)  
 ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

**DEVICE IDENTIFIER MODE**

The Device Identifier Mode allows the reading of a binary code from the EPROM that identifies the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

**M5L27512K DEVICE IDENTIFIER CODE**

Code	Pin	A <sub>0</sub> (10)	D <sub>7</sub> (19)	D <sub>6</sub> (18)	D <sub>5</sub> (17)	D <sub>4</sub> (16)	D <sub>3</sub> (15)	D <sub>2</sub> (13)	D <sub>1</sub> (12)	D <sub>0</sub> (11)	Hex data
Manufacturer code	V <sub>1L</sub>	0	0	0	1	1	1	1	0	0	1C
Device code	V <sub>1H</sub>	0	0	0	0	0	1	1	0	1	0D

Note 5: V<sub>CC</sub> = 5V ± 5%, A<sub>g</sub> = 12.0 ± 0.5V, A<sub>1</sub> ~ A<sub>8</sub>, A<sub>10</sub> ~ A<sub>15</sub>,  $\overline{CE}$ ,  $\overline{OE}/V_{pp}$  = V<sub>1L</sub>

勝特力材料 886-3-5753170  
 勝特力电子(上海) 86-21-54151736  
 勝特力电子(深圳) 86-755-83298787  
[Http://www.100y.com.tw](http://www.100y.com.tw)